ERS 220

Practical report 1:

Binary adder

Group 35

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FORM A

UNIVERSITY OF PRETORIA

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Practical Guidelines

These guidelines must be read and followed by all students. It is expected that a copy of these guidelines be signed by each student and attached to the first practical report. Failure to do so will result in a zero for your practical and report.

1. Please remember this is a DEMO session i.e. your practical must be completed before the assigned time. Do NOT arrive at the session expecting three hours to work on your practical.
2. Every group member MUST have a lab book. Sharing is not permitted i.e. every group must have the respective number of completed lab books. Pro rata of the total for the practical will be deducted for every lab book not present.
3. If you are late for your demo session, as allocated, you will receive zero for the practical. This is not negotiable. If one of your group members fails to arrive they will receive zero, unless for medical reasons or prior arrangements have been made with the lecturer.
4. If your practical does not function correctly during the session you may be allowed a re-demo. This will occur during the next week's practical and will only be given if your group can demonstrate that work was completed on the practical prior to the session and all of your lab books are complete.
5. Your practical report (1 per group) must be handed to your demonstrator at the completion of your demonstration. It must have a cover page, stating your group number clearly, table of contents, plagiarism statement signed by ALL group members, group members who do not sign will receive zero for the report and failure to include a statement will result in the group receiving zero, a signed copy of these guidelines and all the headings listed in the study guide. Failure to hand in a report during the session will result in a zero for the report.
6. When you arrive at the practical session write your chosen bench number under your group number. As you have chosen the bench you will be expected to be at the bench given. Demonstrators will not wonder around the labs trying to find you. If you have not demonstrated your practical during your allocated time you will receive zero. This is not negotiable. If you fail to indicate your bench number your practical will not be marked and you will receive zero.
7. Arrive at least 15-20 minutes before your allocated time to ensure your practical's functionality.
8. Students have not been assigned to benches. As such if you choose a non-functioning bench, change benches. Non-functioning benches will NOT be accepted as an excuse for non-functioning practicals.
9. Each group must complete their own practical. If it is determined that more than one group has demonstrated the same circuit the groups that colluded will receive zero and NOT given the option to re-demo.
10. Students must buy their own components. As such not having correct components is NOT a valid reason to not complete a practical.

Declaration:
I have read and understood these guidelines and will follow them during all practical sessions.

Name:_____ Signature:_____

Name:_____ Signature:_____

Name:_____ Signature:_____

Name:_____ Signature:_____

Name:_____ Signature:_____

Summary

Digital machines need a carefully devised set of instructions, in the form of logic functions, to solve problems of a mathematical or logical nature. To translate those problems into solutions a truth table helps to establish the relationship between input and output and assists in finding the initial logic expressions. The expressions can then be simplified to aid implementation and reduce redundancy by means of tools like Karnaugh Map and switching algebra and Boolean algebra. Intuitive insight can sometimes simplify the circuits even further in the final stages. Logic expressions can be directly transformed into digital circuit. These steps enable us to create truly useful digital circuits to solve problems by enabling us to develop the fundamental instructions, in the form of logic functions; a digital machine requires to operate.

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Introduction

Problem Statement

Computers, or digital machines, are not able to intuitively identify and process data such as mathematical functions. Instead they have to rely on carefully designed fundamental operations based on Boolean algebra. The problem is to translate these functions into the building blocks of digital systems, two states (“hi”, “lo” or ‘1’,’0’) and gates which translate, and combine these states.

Problem Formulation

To investigate how different logic gates work, realize how the use of certain simplification and Boolean-algebra can minimize the amount of gates that is needed to achieve the needed function.

Background

Digital computers can only represent numbers in ‘1’ and ‘0’ so they require a different set of mathematical rules to achieve results. These rules are known as switching algebra or Boolean algebra. Boolean algebra expresses all problems as a combination of true or false events.

A truth table is a table that is used to relate inputs to outputs (event to output events). It is a useful tool for establishing initial logic expressions.

The rules of switching algebra are a set of rules that allow us to algebraically simplify logic expressions.

A Karnaugh maps is a visual tool to help us simplify logic expressions either by direct substitution into the map from a truth table or using overlapping areas indicated on the map to directly map logic expressions.

A seven segment display is a clever arrangement of LED’s that allow a decimal number to be displayed. It can be driven by a simple driver that accepts a binary coded decimal as input, or a normal binary number to be displayed in the hexadecimal form.

The implementation of de-bouncing a switch is to prevent possible undefined or ‘floating’ inputs that could result in undesired outputs and resulting oscillations. The simplest de-bouncing configuration uses a simple circuit with a resistor linked to Vcc and a switch connecting the resistor to ground. A inverter is connected at the node between the resistor and switch. When the switch is open the inverter reads a high voltage, and thus outputs a ‘off’ value. When the switch is closed it shorts out the voltage resulting in a lo detected by the inverter, causing a “on” output. (Reddy, 2011)(Wakerly,2006)

Design and Implementation

Approach

In this Practical various concepts in digital design such as truth tables, Karnaugh maps and Boolean algebra was used to propose and simplify logic expressions to achieve the addition of two, three bit numbers in binary format and to output the result in both binary, as well as the more user friendly form of a seven segment display.

Detailed Design and Implementation

At the onset of solving a problem using a digital system the challenge is to translate the real world problem into a function of Boolean which is then used to deduce a system consisting of logic gates. An old and trusted way of achieving this is a truth table. A truth table lists all possible inputs and relates them to all possible outputs. Although a Boolean expression can be obtained directly from the truth table it will be long and will incorporate possible redundancies. The use of the tool Karnaugh maps was used to simplify these expressions and to eliminate redundancy. The results obtained from the Karnaugh maps are strictly in the form of and, or, and not operators which can be simplified further buy the rules of switching algebra and the incorporation of more complex expressions such as the exclusive OR operator. These expressions of Boolean algebra is the used to draw up a circuit diagram which can be further simplified to eliminate redundancy by combining sections of the circuit common to multiple outputs. These circuits where then built, tested and debugged. Simulations can greatly add to the debugging of circuits.

Results and Discussion of Results

One approach to the design would be to put the complete input of two 3-Bit numbers into the truth table, and simplify from there. Another approach is to split the problem into smaller more manageable parts. If the first two digits of a binary number is considered one would get the first digit of the solution and a possible carry to the next digit (2 inputs, 2 outputs). If we consider the second digit we need to consider the digits been added and the possible carry from the previous digits and get the second digit of the solution and a new carry value (3 inputs, two outputs). All subsequent digits follow in the same way as the second. Let’s call the first digit procedure a half adder and the second digit procedure a full adder. The advantage of such an approach is that these blocs can then be cascaded to form a adder of any bit size (not only a 3-bit adder. It could also form the building blocks of a sequential adder that can use finite hardware to add very large numbers. The cascade method was used.

Truth Table

A truth table was implemented to take into consideration all possible combinations that the input binary variables can take and relate them to the output.

Half adder

Half adder

	A	B	Y	C
0	0	0	0	0
1	0	1	1	0
2	1	0	1	0
3	1	1	0	1

Table 1 Truth table for half adder

The functions for the half adder are immediately visible from the truth table and are in the simplest form as they consist of only one gate per output. Thus further simplification is unnecessary. The logic expressions are as follows:

Y = A (+) B

C = AB

Full adder

Full adder

	A	B	C(in)	Y	C (out)
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

Table 2 Truth table for full adder

This table would produce long redundant expressions for the outputs thus further simplification is necessary.

Karnaugh Map Simplification

Full adder

The following Karnaugh Maps where produced to simplify the full adder truth table and to obtain initial expressions for the full adder.

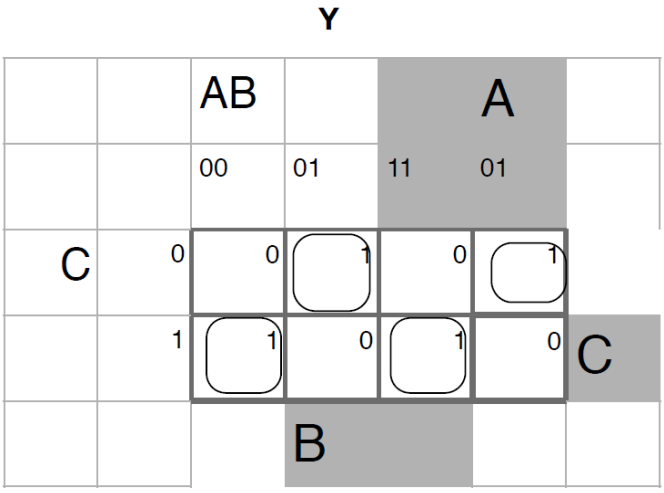


Figure 1 Karnaugh Map for Y

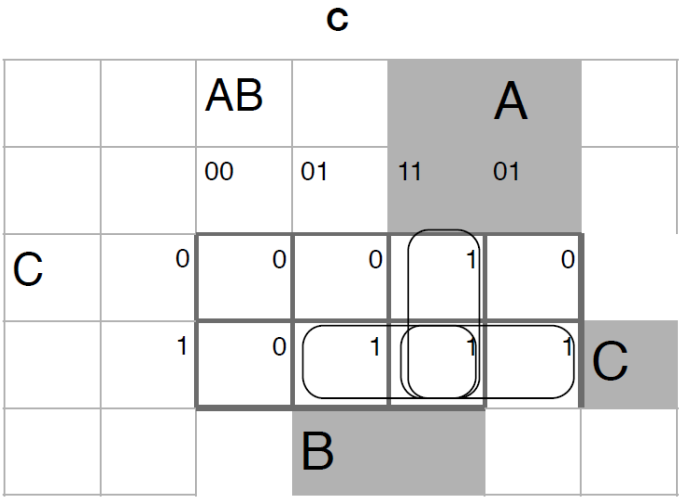


Figure 2 Karnaug map for carry

The following expressions for the outputs are obtained from the Karnaugh Maps:

Y= AB'C+ABC+A'BC'+ A'B'C

C = AB+BC +AC

Simplification by application of switching algebra

Full adder

The rules of switching algebra were used to minimize the expressions to the simplest state.

Y= AB'C+ABC+A'BC+ A'B'C	C(out)= AB+BC +AC
(AB'+A'B)C'+(AB+A'B')C	AB(C'+C)+AC(B'+B)+BC(A'+A)
(AB'+A'B)C'+((A'+B')'+(A+B)')C	ABC'+~~ABC~~+AB'C+~~ABC~~+A'BC+ABC
(AB'+A'B)C'+((A'+B')(A+B))'C	ABC'+AB'C+A'BC+ABC
(AB'+A'B)C'+(~~A'A~~+A'B+AB'+~~B'B~~)'C	(A'B+AB')C+AB(C'+C)
(AB'+A'B)C'+(A'B+AB')'C	(A(+)B)C+AB
(A(+)B)C'+ (A(+)B)'C	
(A(+)B)(+)C	

Elimination of common parts

It is easily observed that the inner function X = (A(+)B) is common to both Y and C(out). It is shown later how this is used to further simplify the on circuit level.

Circuit Schematic

Half adder

The following circuit can be deduced for the half adder:

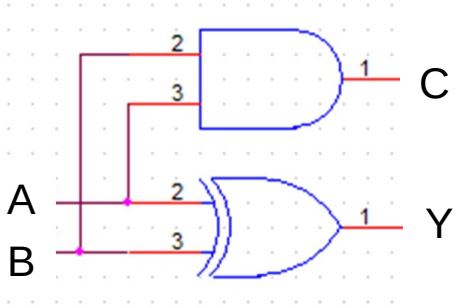


Figure 3 Half adder

Full adder

The following circuit can be deduced for the full adder:

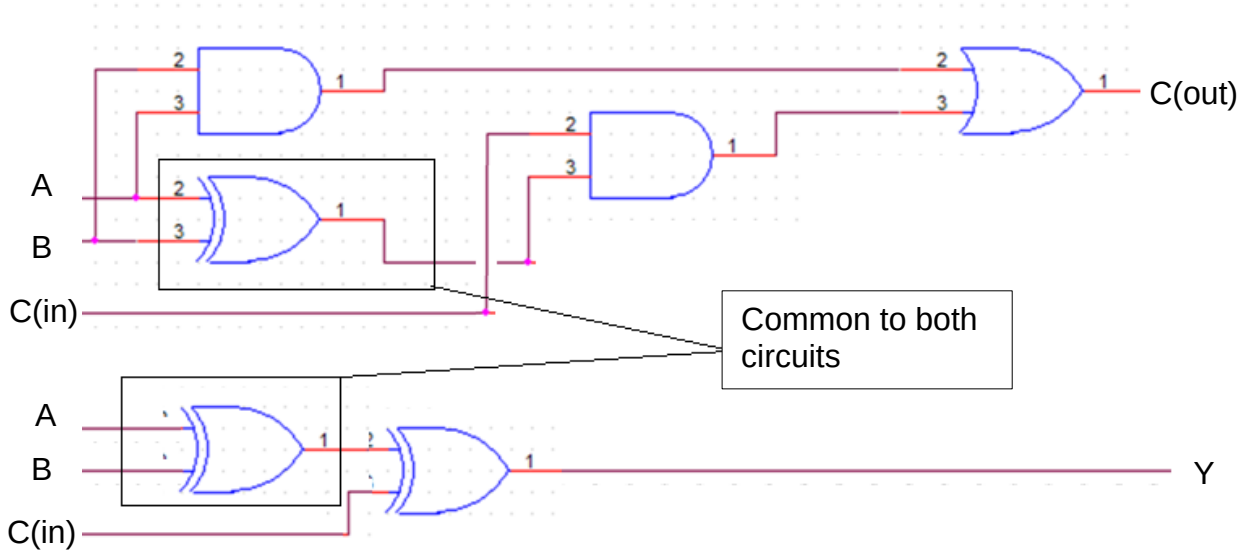


Figure 4 Full adder

As shown above there is a gate in common to both circuits. We can combine these circuits to eliminate the duplication.

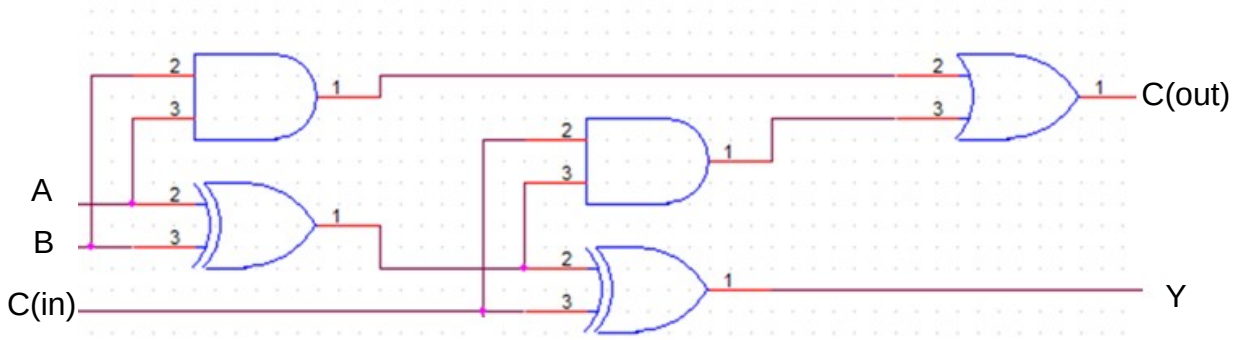


Figure 5 Full adder (simplified)

3-bit adder

The complete logic circuit is shown below.

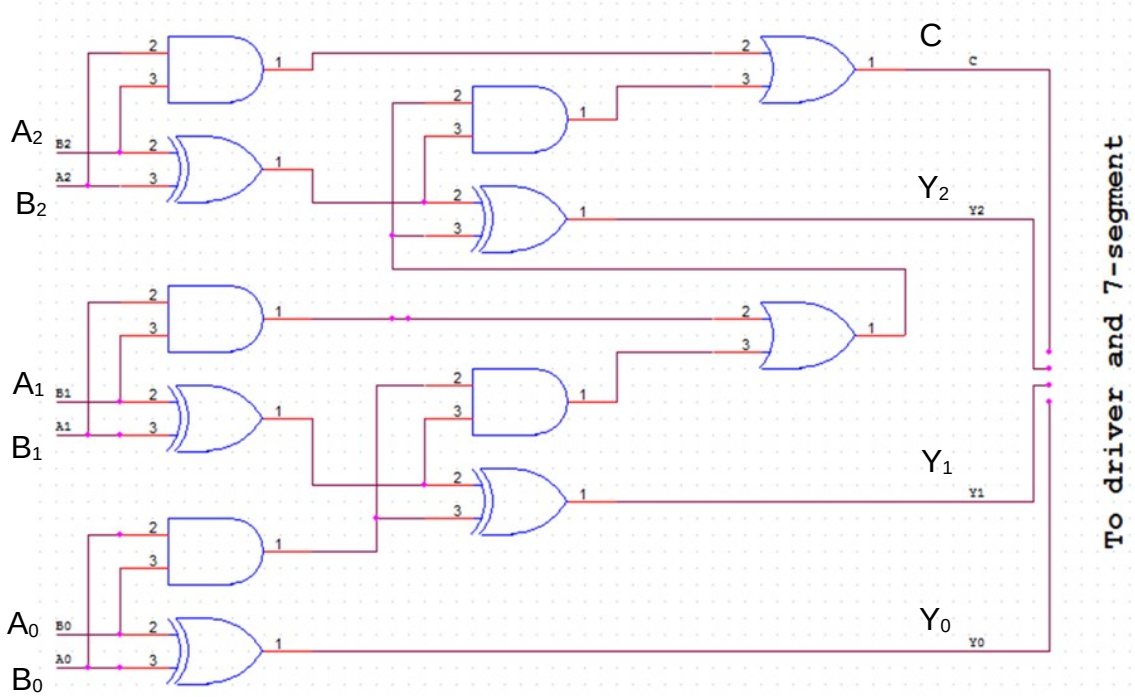


Figure 6 Three bit adder

The input was generated using dip switches, denounced using a resistor link and inverter configuration. The final output is fed into a driver that displays the output in decimal form on a seven segment display.

Conclusion

This design clearly illustrates the ability of digital systems to solve problems and functions if the correct procedures are followed to achieve the correct logic expressions (i.e. carefully designed instructions for the machine). The power of Karnaugh maps and switching algebra in the simplification of expressions and the elimination of redundancy was clearly illustrated. In addition to this it was shown that there is still place for intuitive simplification and elimination of redundancy especially in the final stages of the design.

References

1. Reddy, S. 2011. *Study Manual, Digital Systems.* University of Pretoria
2. Wakerley, J.F. 2006. *Digital Design, Principles and practices* Pearson, Pretence Hall