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Department of Electric, Electronic and Computer Engineering

Stochastic Communications
ESC 320

Pre-report

Experiment 3: Symbol Synchronization

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Topic of work: **Experiment 2: Baseband Communication System with Deferential Encoding and Nyquist Filter Design**

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Experiment 3

Symbol Syncronization

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Abstract—This is preparation to perform a laboratory experiment on symbol synchronization. It is a continuation of experiment 2 showing how to recover the clock signal from the data rather than transmitting a separate clock signal.

Index Terms— bipolar signaling, clock recovery, differential encoding, phase lock loop (PLL), symbol synchronization, voltage controlled oscillator (VCO), zero crossing detector

I. Introduction

In continuation of the discussion of baseband communication systems from experiment on , this experiment looks at how to synchronize the clock at the receiver side of such a communication system so that the signal may be sampled at the right instant and that decoding could take place.

An inherent property of using a differentially encoded bipolar signal is that it contains in the data signal sufficient spectral elements at the clock frequency for us to be able to extract the original clock from this signal. This is because a bipolar signal contains no dc elements especially when differential encoding is used to break down any long sequences.

In this experiment it shall be explored how to construct a circuit that would detect the instances of zero crossings and use this to drive a phase lock loop circuit that would lock onto the frequency of the zero crossings thus recovering the original signal. This signal is then used as a clock to drive the sampling decoding and recovery of the received signal.

In this experiment most of the circuit used in experiment one is reused with the addition of the alredy mentioned zero crossing detector and phase lock loop circuit

The experiment two system was designed to condition a non-return to zero (NRI) bipolar signal for optimal transmission at a bit rate of 16 kilobits per second. The signal was prepared for transmission using differential encoding (to reduce long DC sequences) and Nyquist filtering (to reduce inter symbol interference).

II. Theory

A. Zero Crossing Detector

The purpose of the zero crossing detector is to produce a narrow pulse every time the received signal crosses 0 volts. This then produces a train of narrow pulses at the original clock frequency for the phase lock loop to lock on to. To achieve this in principal we take a phase delayed sign and correlate it to the original signal, at the zero crossing these signals should have a high correlation. This is because if we compare the signal just after it the zero crossing and just before the next crossing we find that this is indeed very similar as the one pulse is still rising and the other is decaying at, assuming the pulse shaping is symmetrical. Hence we

should design a circuit capering the received signal compared to a signal Delayed by where delta is much smaller than the sampling interval T. correlation at points other than the zero crossing would yeald a low correlation. In practice we would replace the correlation process by XOR function.

B.Phase Lock Loop

A phase lock loop (PLL) consists of 4 parts, a voltage controlled oscillator (VCO), low-pass filter and feedback path and, a phase comparator. The VCO could be achieved with colpits or clap oscillator or simply using the laboratory bench signal generator with a tracking function, the PLL functions by comparing the phase of the input signal and the output signal via the feedback circuit and adjusting the input to the VCO passed on the phase difference, we thus say that the PLL tracks the phase of the input signal. The PLL remains stable even with jitter and variation in timing making it ideal as the decoding clock is then matched to the delayed and distorted data and not a local clock, making for more ideal sampling and immunity to timing jitter.

The PLL is specified in terms of type and order, hold-in range, pull-in range, and lock in range. For this practical the type would be an analog second order PLL. It is to have a center frequency 16khz with a bandwidth of +-200Hz so a lock range from 15800Hz to 16200Hz

III. Design

A. Zero Crossing Detector

For a zero crossing detector either a filter or a cascade of digital devices can be used to achieve a phase delay as shown in figure 1 and, figure 2.

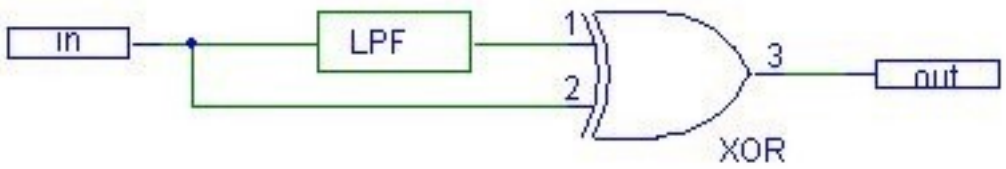


Fig. 1 Filter delay zero crossing detector

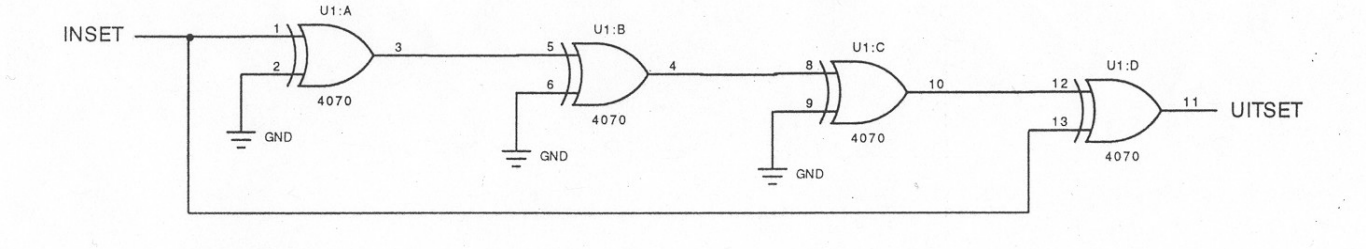


Fig. 2 Cascaded XOR zero crossing detector

B.Phase Lock Loop

For a second order PLL the loop filter frequency can be calculated using this formula

F(s)=, where $\tau 1=R_1C$ *and* $\tau 2=(R_1+R_2)C$ this will be combined with the bench signal generator as VCO and a XOR gate a phase comparator.

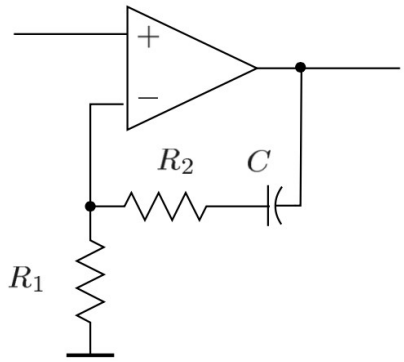


Fig. 3 Loop Filter

IV. Discussion

Using these designs the clock frequency can be effectively recovered and the signal decoded restoring it to the original signal without the need to transmit the clock independently.

V. Conclusion

Recovering the clock frequency from the bipolar differentially encoded signal using a zero crossing detector has the following benefits;

1. It eliminates the need to transmit a clock eliminating the need for additional channels or bandwidth
2. It improves robustness with regards to timing jitter and phase distortions that could influence the optimal sampling point.

References

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